FIG. 1
PRIOR ART

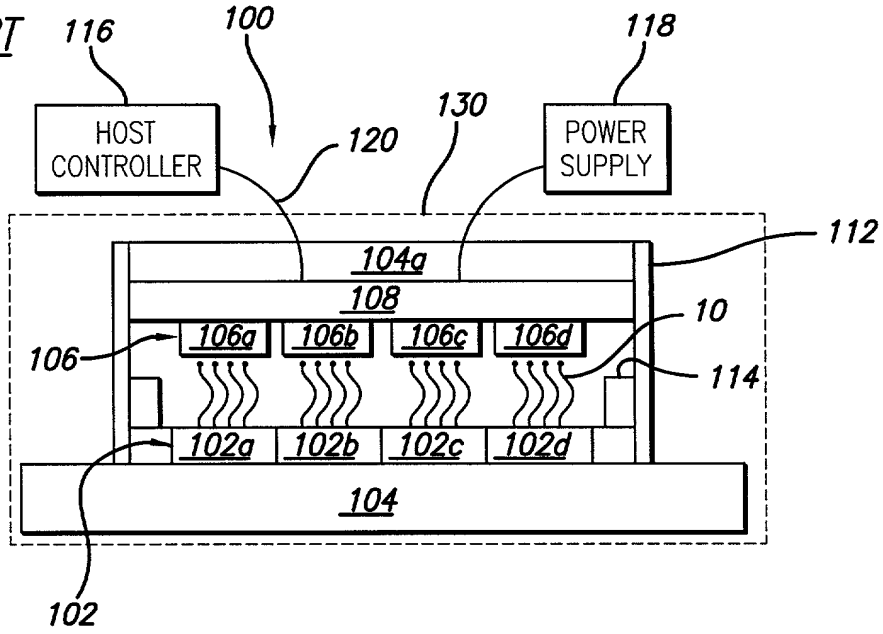


FIG. 2
PRIOR ART

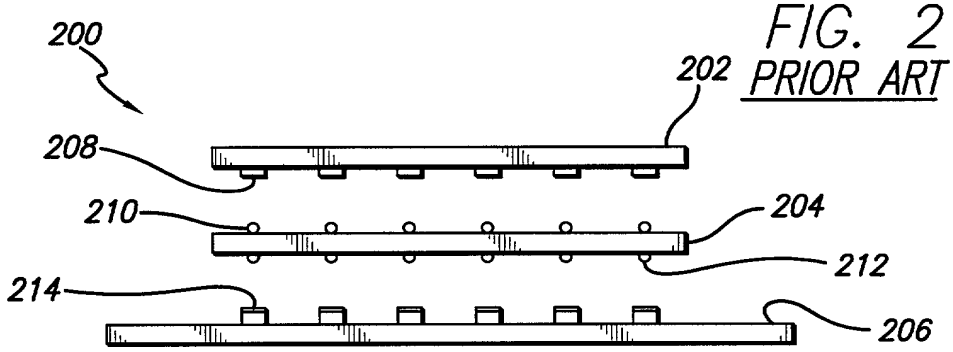


FIG. 3a

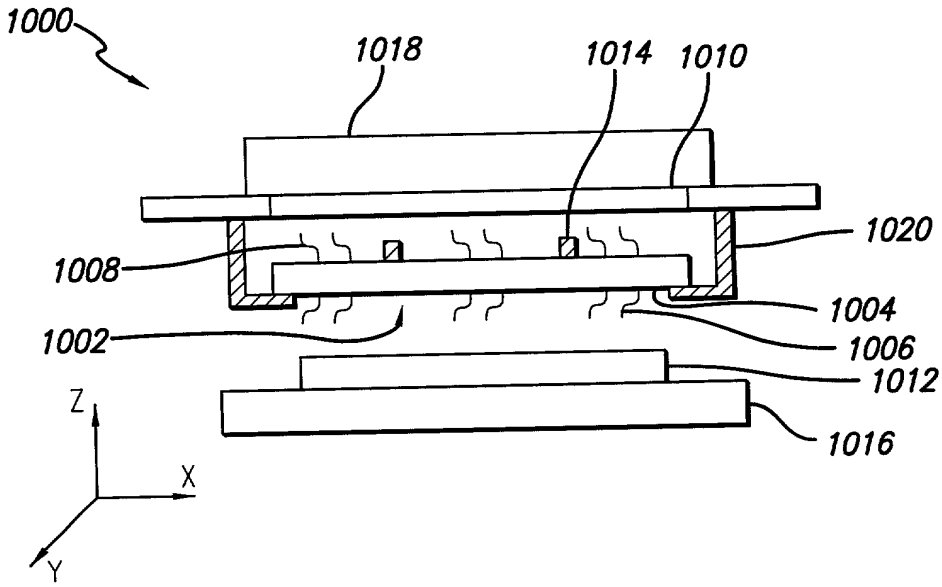

1000
1018
1014
1010
1020
1008
1004
1002
1006
1012
1016
Z
X
Y

FIG. 3b

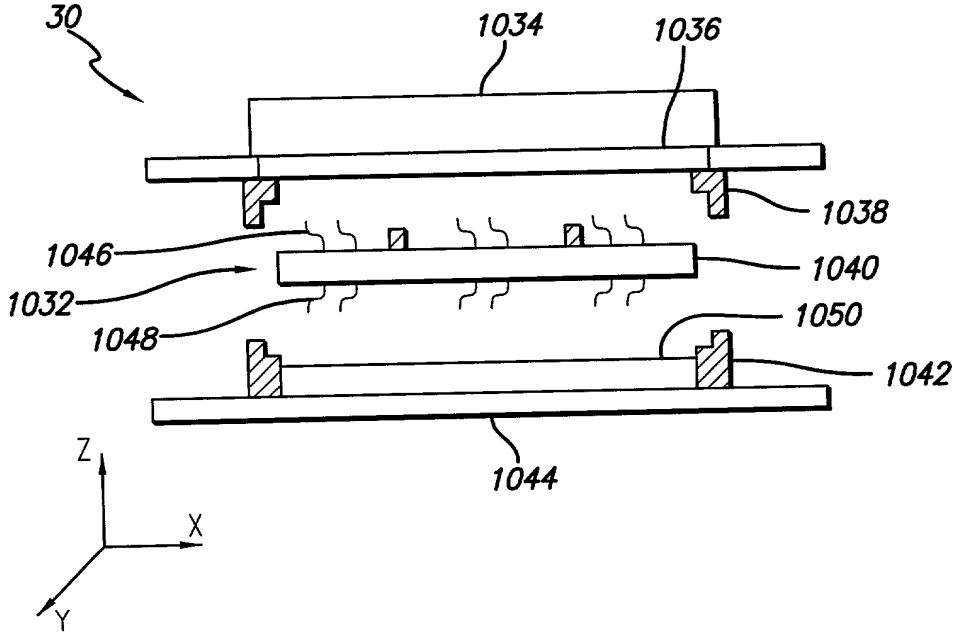

30
1034
1036
1038
1046
1040
1032
1050
1048
1042
1044
Z
X
Y

FIG. 4a

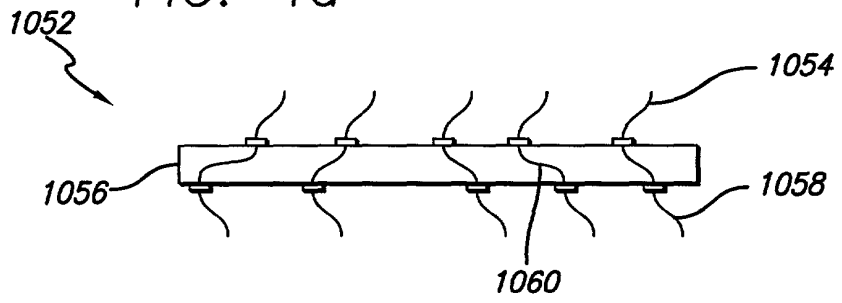


FIG. 4b

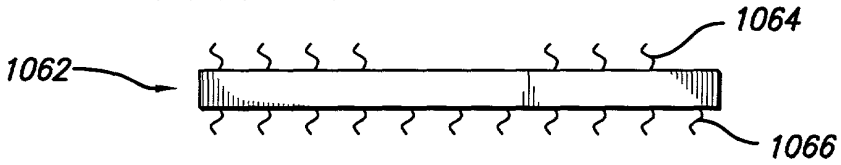


FIG. 4c

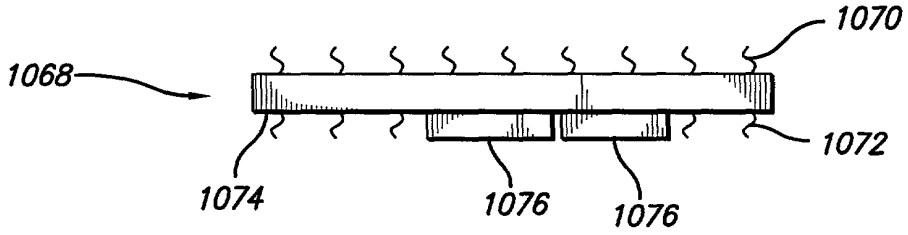


FIG. 4d

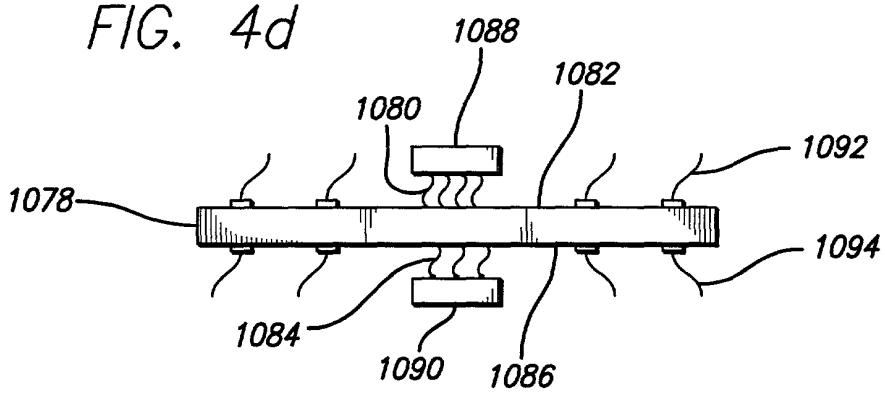
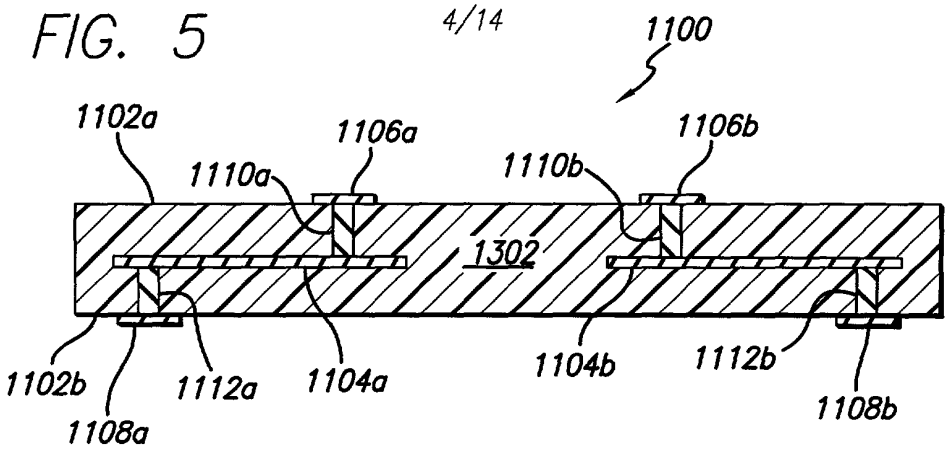


FIG. 5



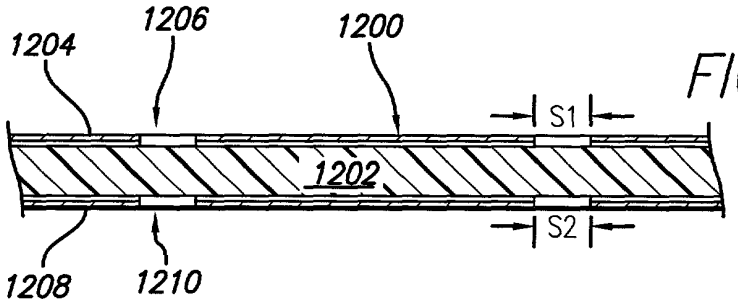


FIG. 6a

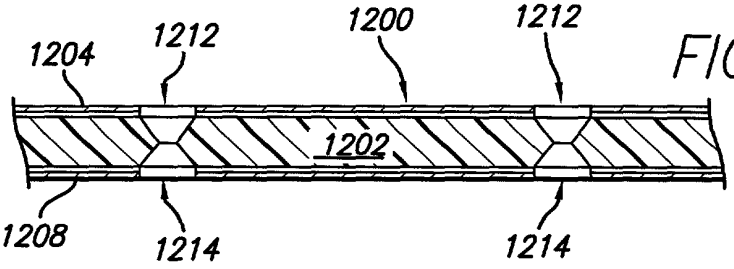


FIG. 6b

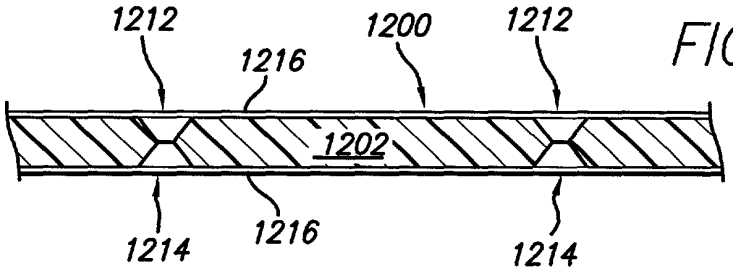


FIG. 6c

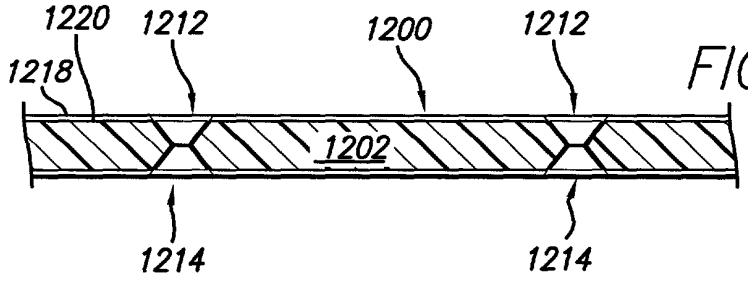


FIG. 6d

FIG. 6e

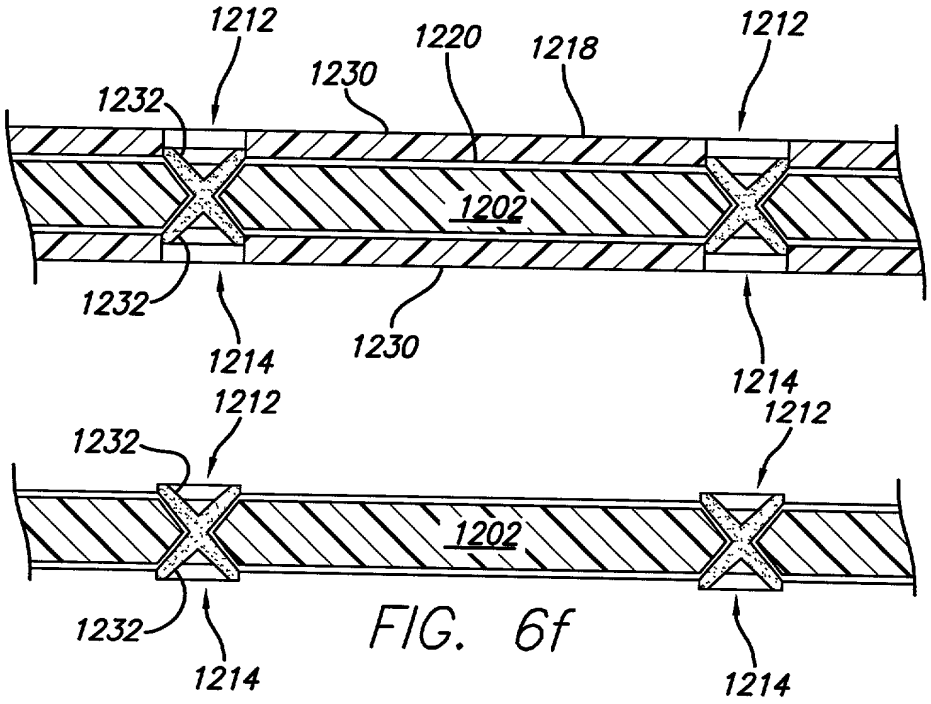


FIG. 6f

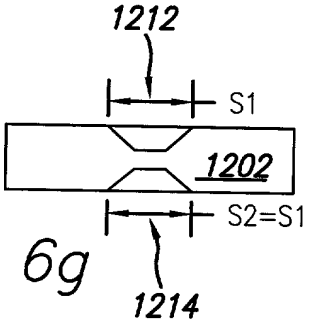


FIG. 6g

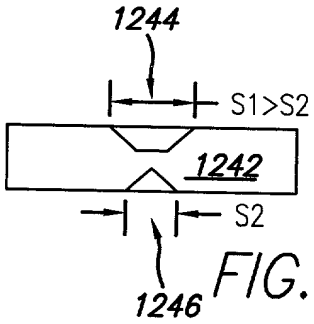


FIG. 6h

FIG. 6i

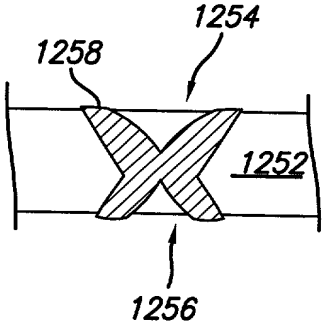


FIG. 7a

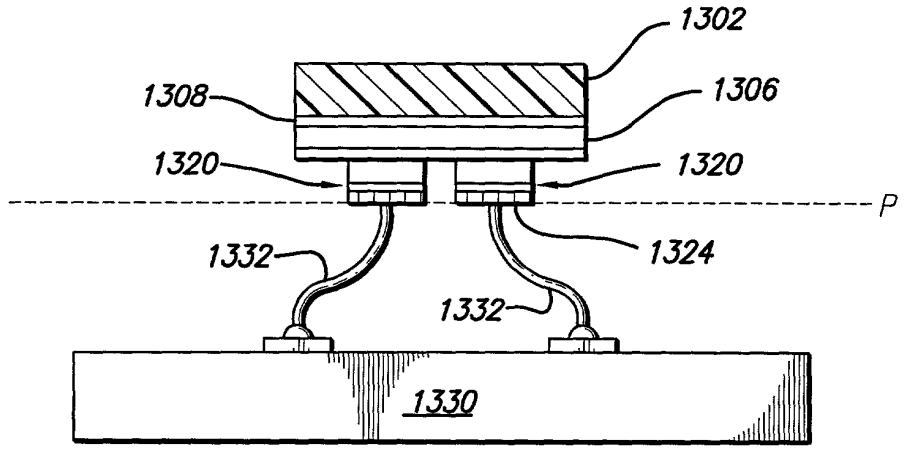

1302
1308
1306
1320
1320
P
1332
1324
1332
1330

FIG. 7b

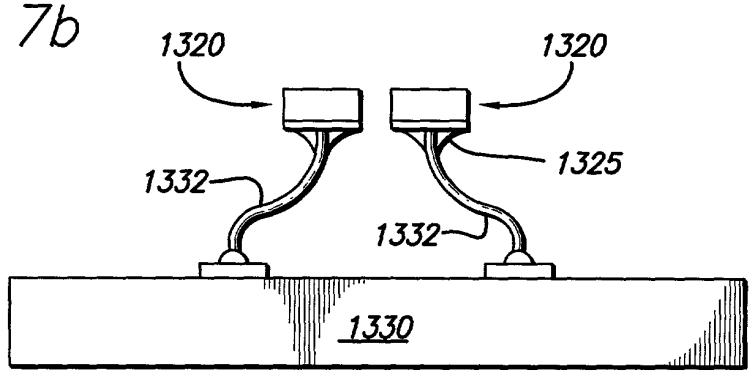

1320
1320
1325
1332
1332
1330

FIG. 8a

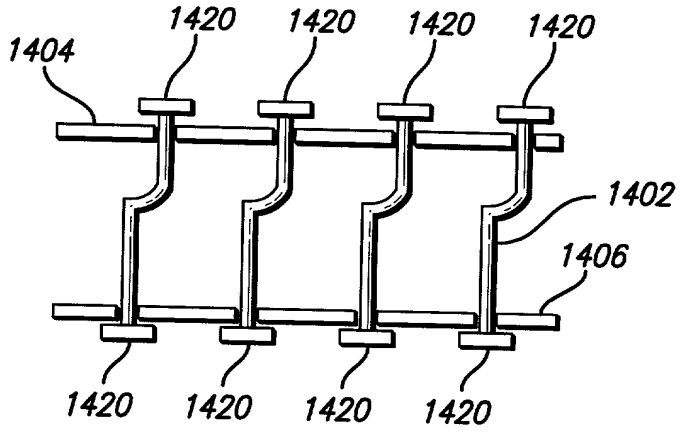


FIG. 8b

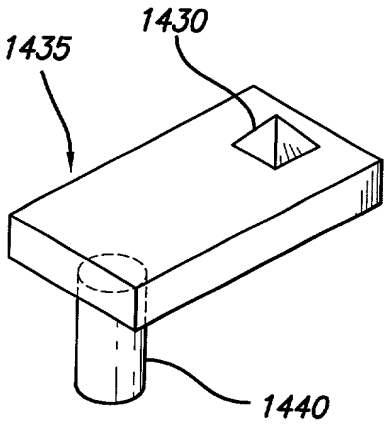


FIG. 8c

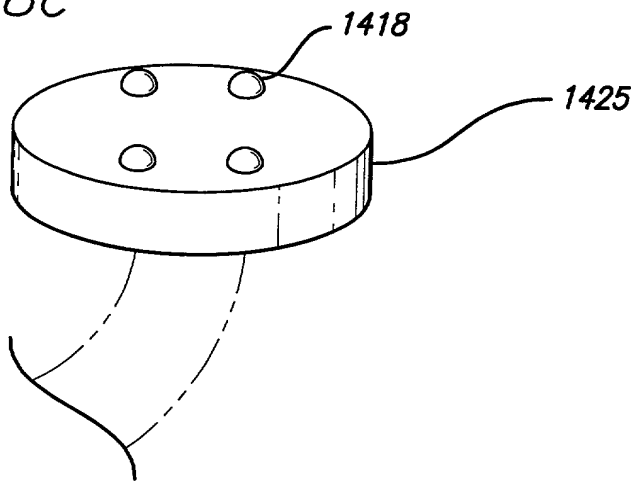


FIG. 9a

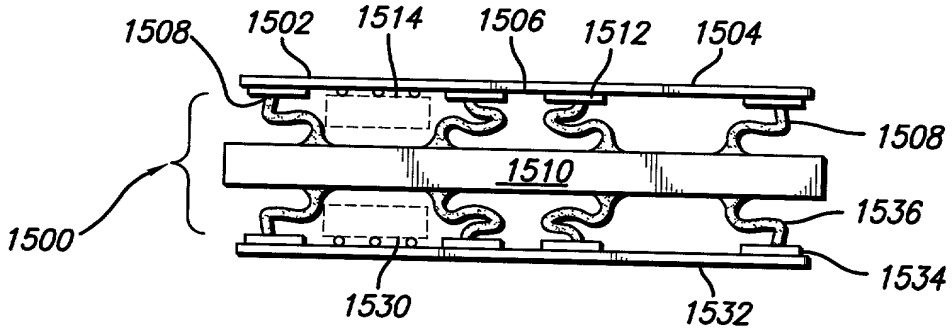

1508
1502
1514
1506
1512
1504
1508
1510
1500
1536
1534
1530
1532

FIG. 9b

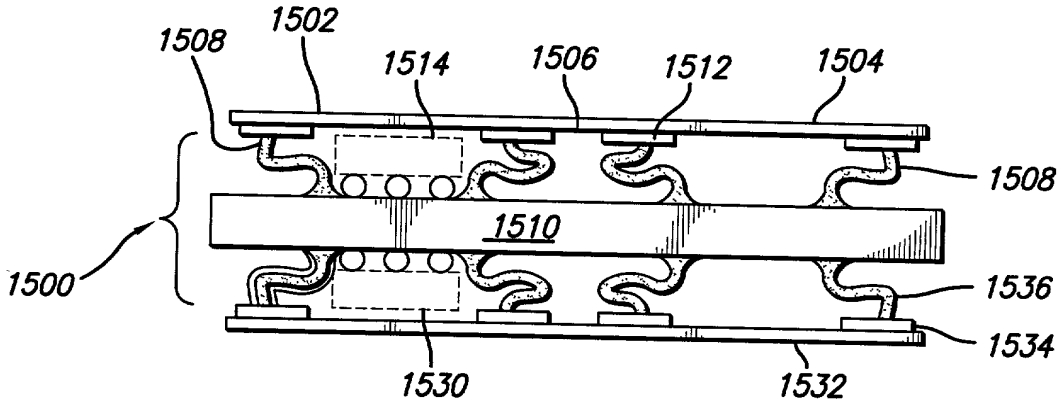

1508
1502
1514
1506
1512
1504
1508
1510
1500
1536
1534
1530
1532

FIG. 10a

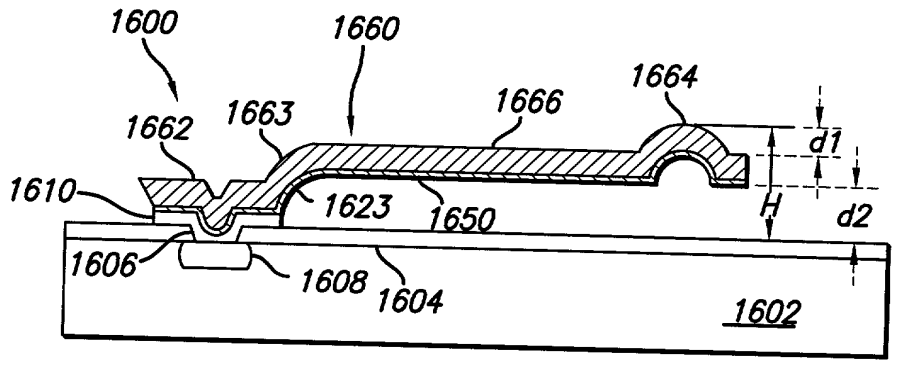


FIG. 10b

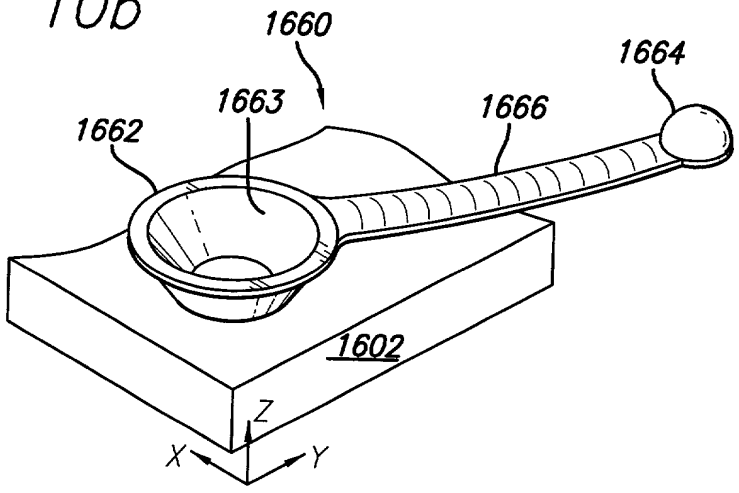


FIG. 11

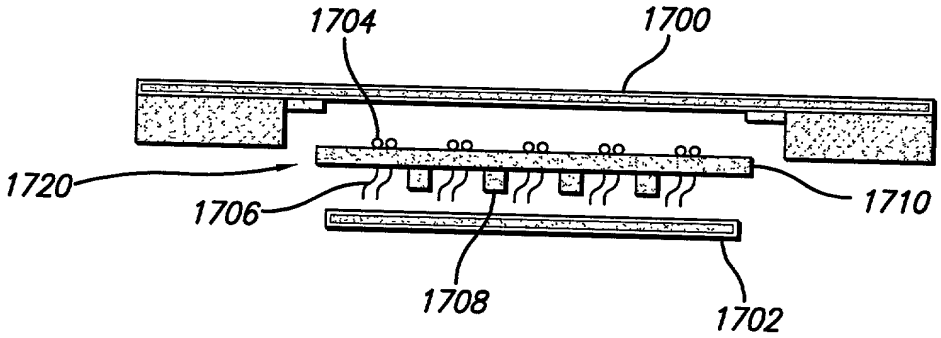


FIG. 12

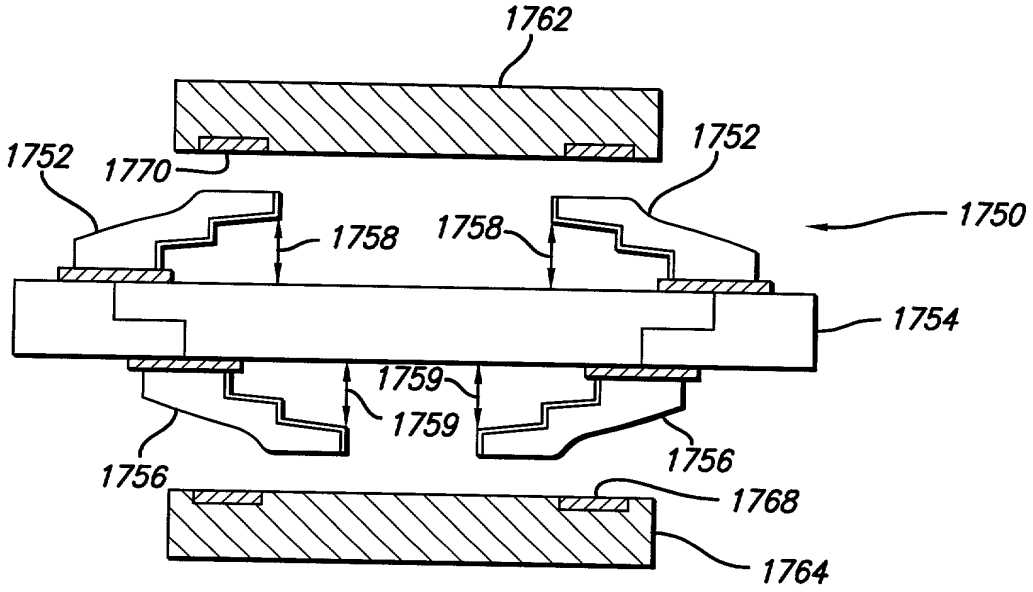
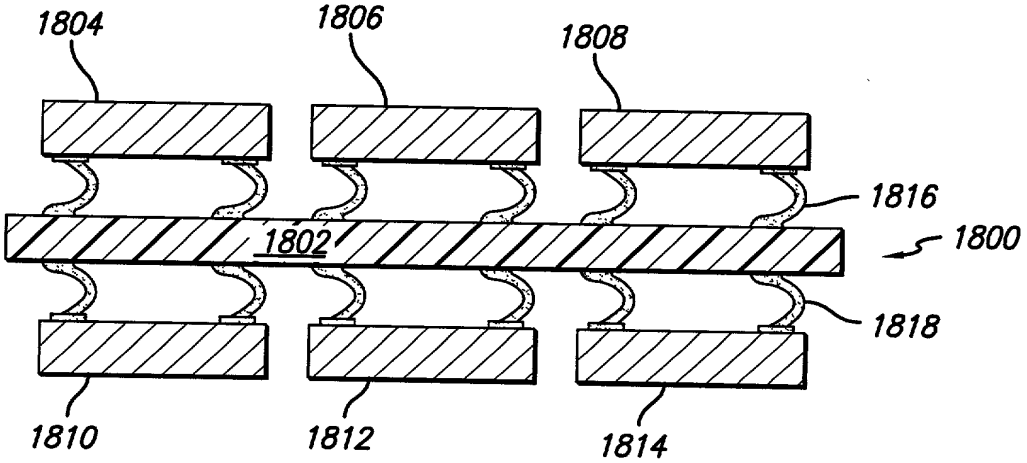

1762
1752
1770
1752
1750
1758
1758
1754
1759
1759
1756
1756
1768
1764

FIG. 13


1804
1806
1808
1816
1802
1800
1818
1810
1812
1814

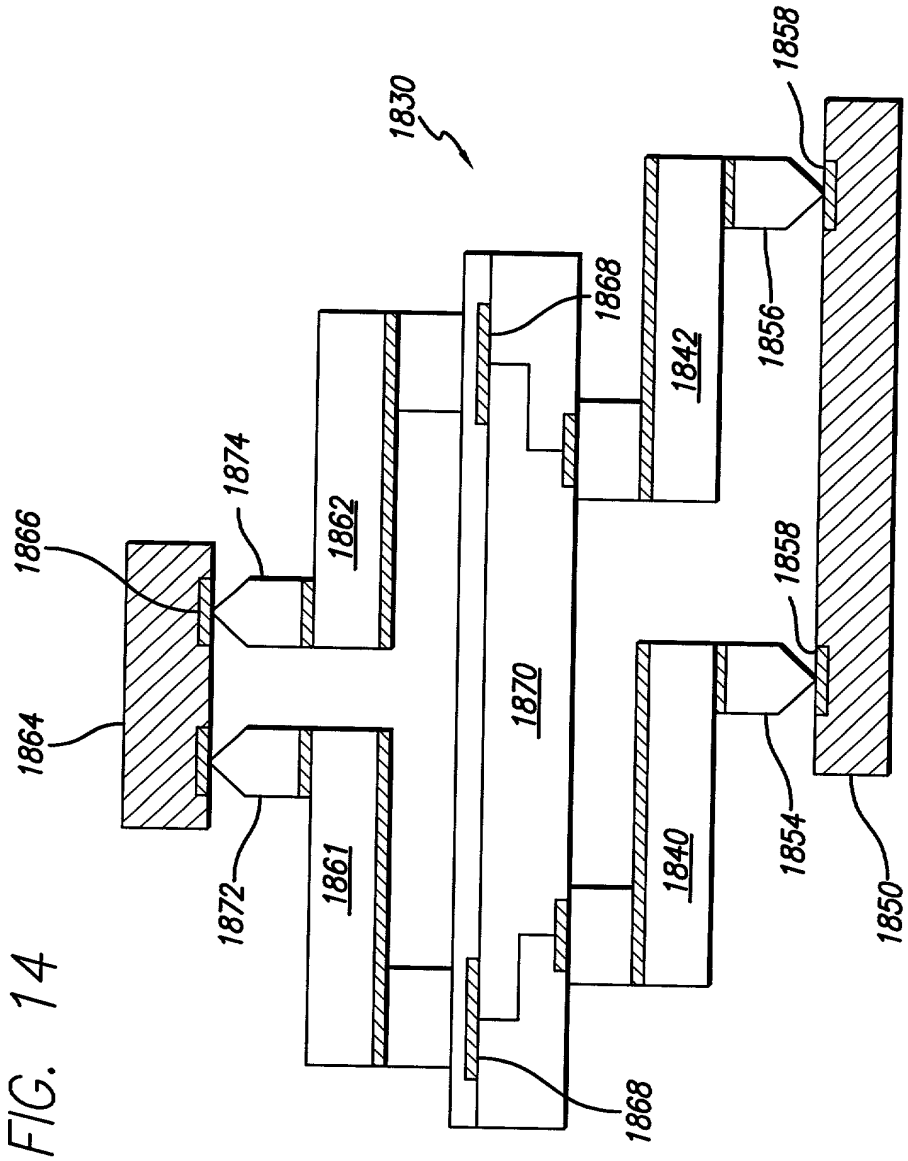

1830
1858
1868
1856
1842
1874
1866
1862
1858
1870
1864
1854
1872
1861
1840
1850
1868

FIG. 14

FIG. 15

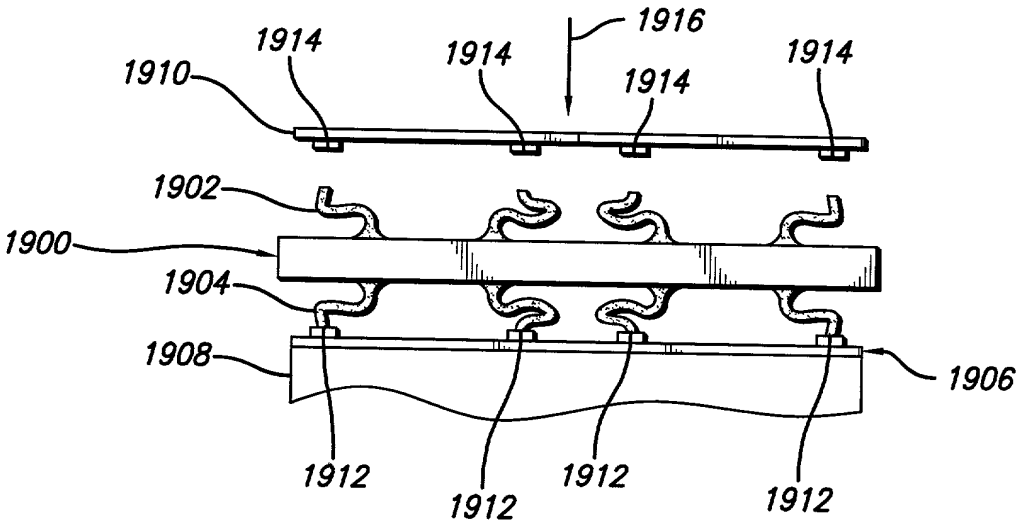

1916
1914
1914
1914
1914
1910
1902
1900
1904
1908
1906
1912
1912
1912
1912

FIG. 16

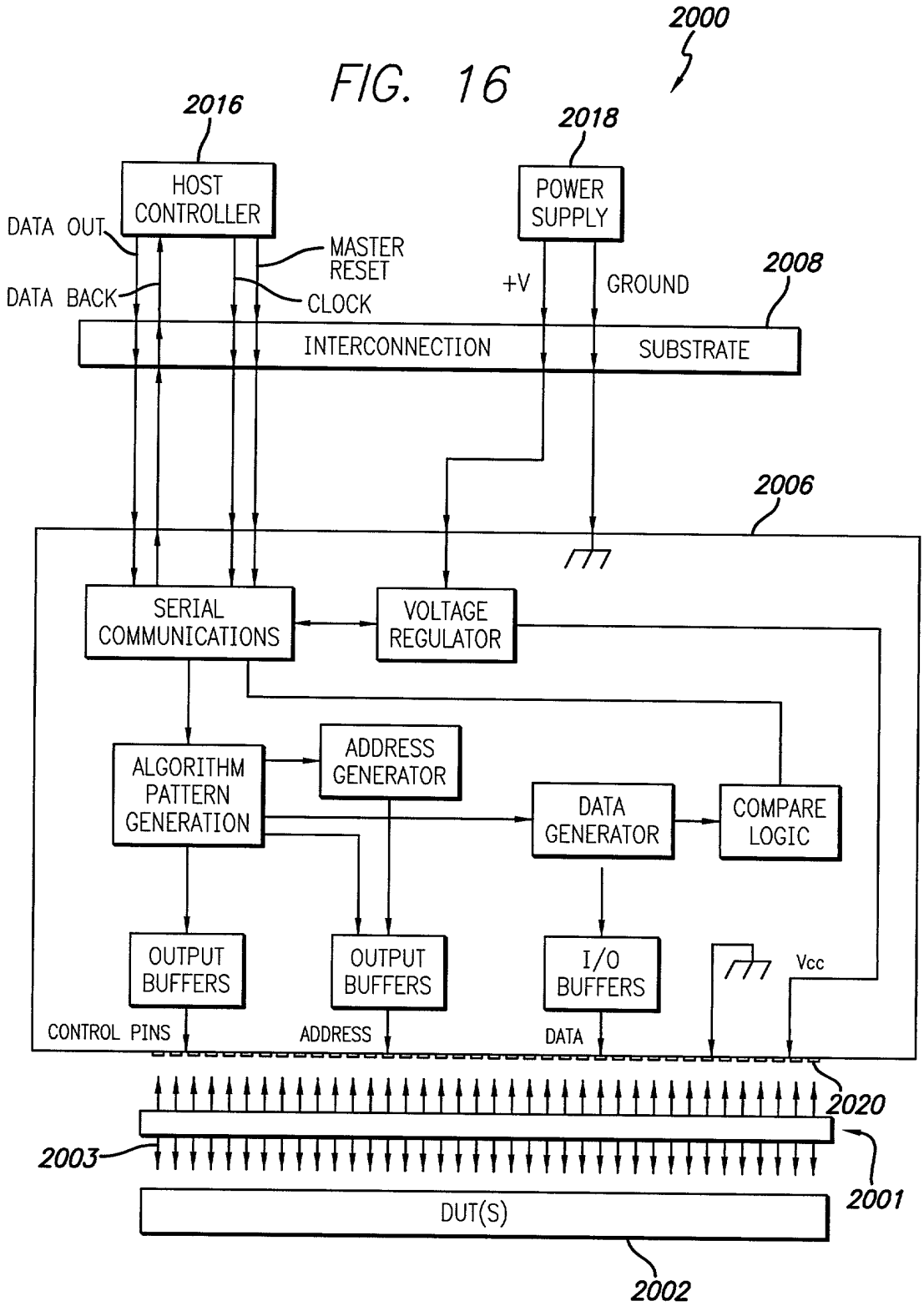

2000
2016
2018
HOST CONTROLLER
POWER SUPPLY
DATA OUT
MASTER RESET
DATA BACK
CLOCK
+V
GROUND
2008
INTERCONNECTION
SUBSTRATE
2006
SERIAL COMMUNICATIONS
VOLTAGE REGULATOR
ALGORITHM PATTERN GENERATION
ADDRESS GENERATOR
DATA GENERATOR
COMPARE LOGIC
OUTPUT BUFFERS
OUTPUT BUFFERS
I/O BUFFERS
Vcc
CONTROL PINS
ADDRESS
DATA
2020
2003
2001
DUT(S)
2002

FIG. 17

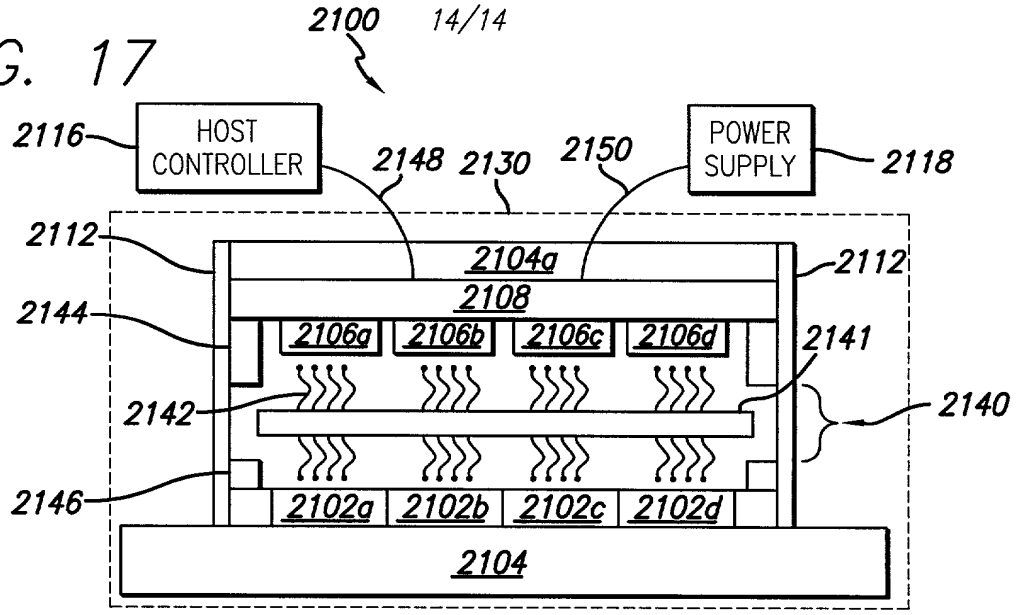


FIG. 18a

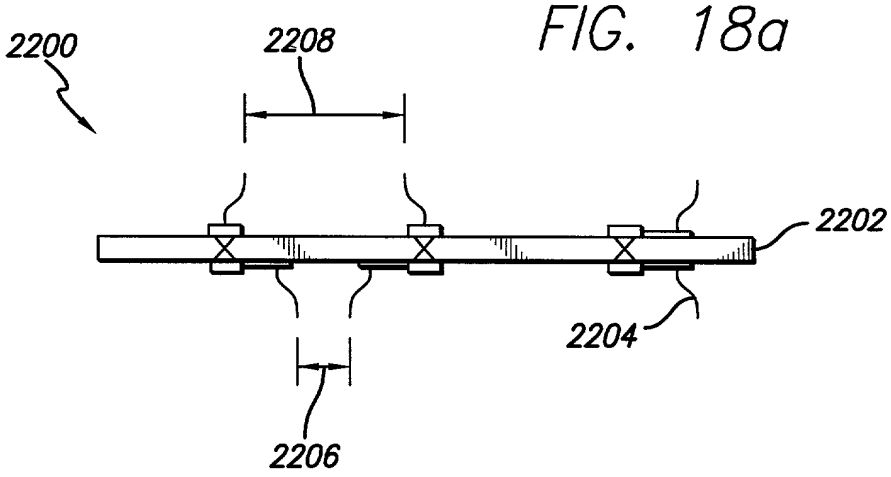


FIG. 18b